

PM-SV32A  
Semiconductor Memory  
Manual



**Plessey  
Peripheral  
Systems**

# PM-SV32A

## Semiconductor Memory

### Manual

November 1978 -- Revision A

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# Section 1

## General Information

### 1.0 INTRODUCTION

This manual provides the information needed to install and operate the PM-SV32A semiconductor memory module manufactured by Plessey Peripheral Systems, Irvine, CA 92714.

The material is arranged into the following sections:

- Section 1 - General Information

This section contains a brief, general description of the PM-SV32A and the specifications of the memory module.

- Section 2 - Installation

This section explains the procedures for equipment installation, including jumper and switch settings.

- Section 3 - Functional Description

This section contains a detailed, functional description of the PM-SV32A address selection, refresh electronics, modes of operation, and interfacing.

- Drawing Package - MD 701660

A separate drawing package is available. This document contains logic diagram, schematics, and assemblies required for a complete understanding of the chassis and power supply.

### 1.1 GENERAL DESCRIPTION

The PM-SV32A is a 32K word MOS dynamic semiconductor memory designed to operate in the DEC LSI-11 Q-bus.\* The memory module is contained on a standard dual board.

\*DEC and LSI-11 are registered trademarks of Digital Equipment Corporation.

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The PM-SV32A is available in four configurations. They are:

<u>Plessey Part Number</u>	<u>Configuration</u>
701660-100	32K x 16 bits
701660-101	24K x 16 bits
701660-102	16K x 16 bits
701660-103	8K x 16 bits

## 1.2 SPECIFICATIONS

### 1.2.1 Electrical

Access Time	250ns	
Cycle Time	500ns	
Power Requirements	+ 5VDC	1.2A
	+12VDC	0.3A

### 1.2.2 Physical

The PM-SV32A is a standard dual height board.

### 1.2.3 Environmental

Temperature:

Storage	-40°C to 85°C
Operating	0°C to 50°C

Relative Humidity: 95% without condensation

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# Section 2

## Installation

### 2.0 INTRODUCTION

This section provides information for the installation and operation of the PM-SV32A bootstrap ROM module.

### 2.1 UNPACKING AND INSPECTION

The PM-SV32A is shipped in a special packing carton designed to keep the board from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the memory requires reshipment.

To unpack the memory, remove any packing materials and visually inspect for physical damage.

### 2.2 INSTALLATION

See Figure 2-1 for switch locations.

### 2.3 REFRESH SWITCH SETTINGS

The PM-SV32A offers two switch selectable refresh modes. External refresh mode is under the control of the processor microcode or user selected DMA device. When external refresh is used on the PM-SV32A, it is usually switch selected to do refresh reply. Only one memory should respond with refresh reply and any memories that are faster during refresh than the PM-SV32A should not be selected for this function.

Internal refresh is accomplished by on-board refresh circuitry. The PM-SV32A refresh is transparent to the processor. Switch SW2 functions are defined in Table 2-1.

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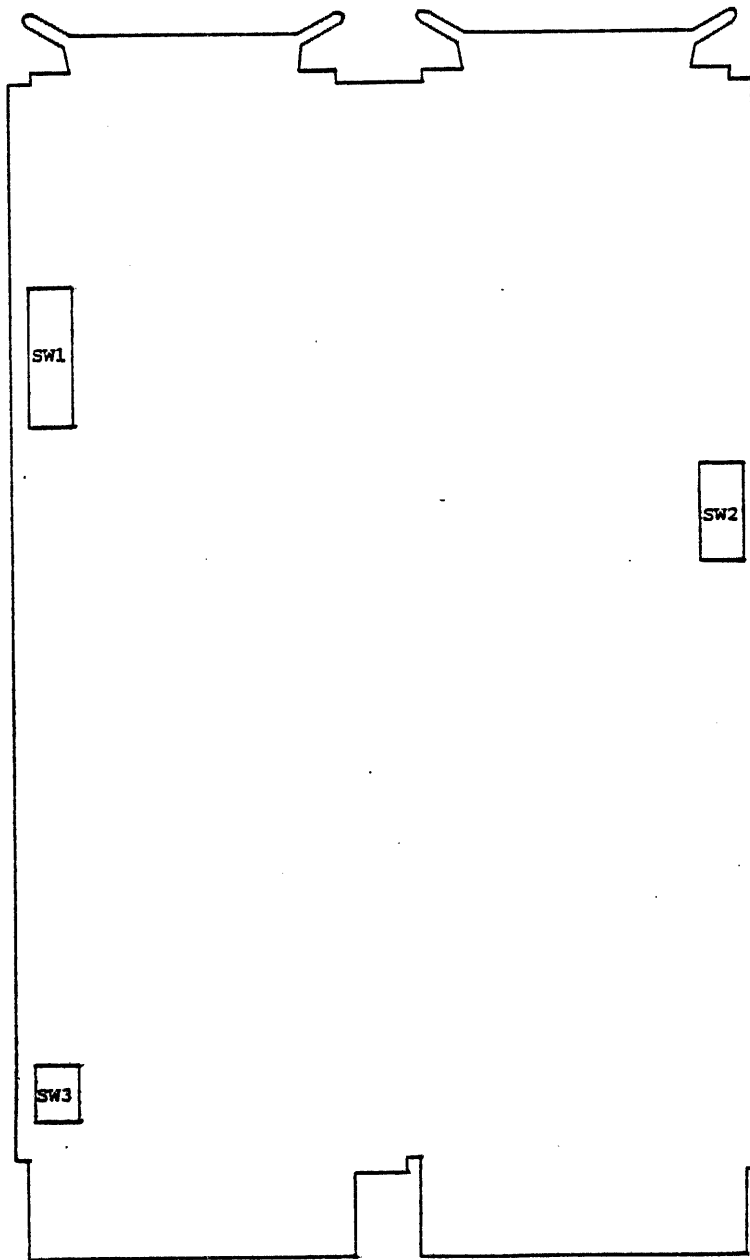


Figure 2-1: Switch Locations (Component Side)

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SW2 POSITIONS	FUNCTION
1	ON - Disable Internal Refresh
2	ON - Disable External Refresh
3	ON - Enables Refresh Reply
4	See Table 2-2.
5	See Table 2-2.

Table 2-1: SW2 Functions

## 2.4 ADDRESS SWITCH SETTINGS

The PM-SV32A is address switch selectable on 4K boundaries. Table 2-2 defines the DIP switch settings for address selection. Table 2-3 defines extended memory switch settings.

ADDRESS SELECTION			SWITCH SETTINGS													
VERSION	SIZE	MEMORY ADDRESS	S1										S2			
			1	2	3	4	5	6	7	8	9	10	4	5		
-100	32K	0 - 28K	ON	ON	ON	ON	ON	ON	ON	ON	X	X	X	ON	X	
-101	24K	0 - 24K	ON	ON	ON	ON	ON	ON	ON	X	X	X	X	ON	ON	
		4 - 28K	X	ON	ON	ON	ON	ON	X	X	X	ON	ON	ON		
-102	16K	0 - 16K	ON	ON	ON	ON	X	X	X	X	X	X	X	ON	X	
		4 - 20K	X	ON	ON	ON	X	X	X	ON	X	X	ON	X		
		8 - 24K	X	X	ON	ON	X	X	X	ON	ON	X	ON	X		
		12 - 28K	X	X	X	ON	X	X	X	ON	ON	ON	ON	X		
-103	8K	0 - 8K	ON	ON	X	X	X	X	X	X	X	X	X	X	*	
		4 - 12K	X	ON	ON	X	X	X	X	X	X	X	X	X	*	
		8 - 16K	X	X	ON	ON	X	X	X	X	X	X	X	X	X	*
		12 - 20K	X	X	X	ON	X	X	X	ON	X	X	X	X	X	*
		16 - 24K	X	X	X	X	X	X	X	ON	ON	X	X	X	X	*
		20 - 28K	X	X	X	X	X	X	X	X	X	ON	ON	X	*	

X = Off

\* = Does not care

Table 2-2: Address Selection Switch Settings

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MEMORY ADDRESS	SW3 SWITCH SETTINGS			
	1	2	3	4
0 - 28K	ON	OFF	OFF	OFF
0 - 29K	OFF	ON	ON	OFF
0 - 30K	OFF	OFF	ON	OFF
0 - 31K	OFF	OFF	OFF	ON

Table 2-3: Extended Memory Switch Settings

## 2.5 POWER REQUIREMENTS

The PM-SV32A is designed to operate on +12V and +5V power supplies and can be operated in a battery back-up mode. The typical and worst case power requirements are shown in Table 2-4. Refer to Figure 2-2 and 2-3 for battery back-up configuration.

VOLTAGE	TYPICAL OPERATING CURRENT	WORST CASE OPERATING CURRENT	BATTERY BACK-UP STANDBY (REFRESH ONLY)
+5V	1.2A	1.6A	1.2A
+12V	0.3A	0.5A	0.25A

Table 2-4: Power Requirements

For battery back-up, do the following:

Cut etch:

<u>CONNECTOR PIN</u>		<u>E#</u>	<u>ADD JUMPERS:</u>
AD2	to	E2	E2 to E3
BD2	to	E8	E8 to E4
AA2	to	E1	E1 to E5
BA2	to	E7	E7 to E6

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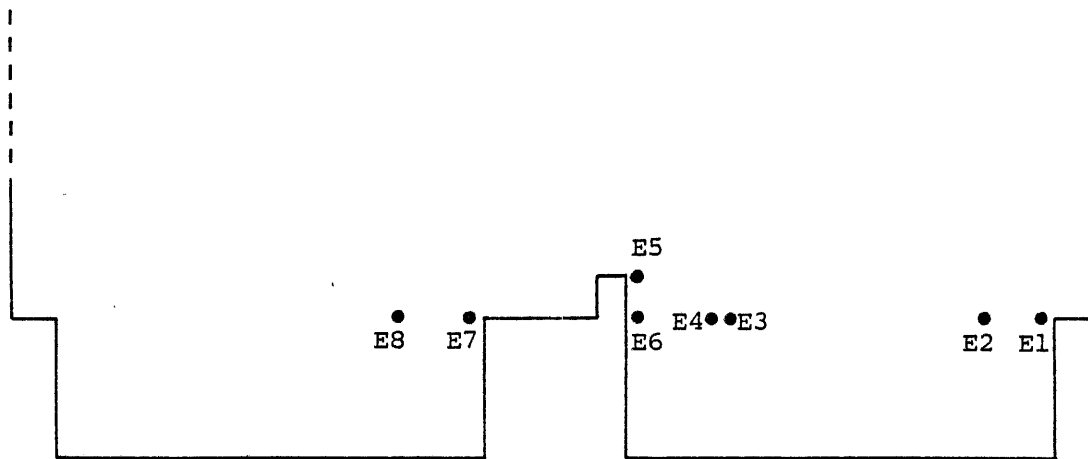


Figure 2-2: Component Side 1

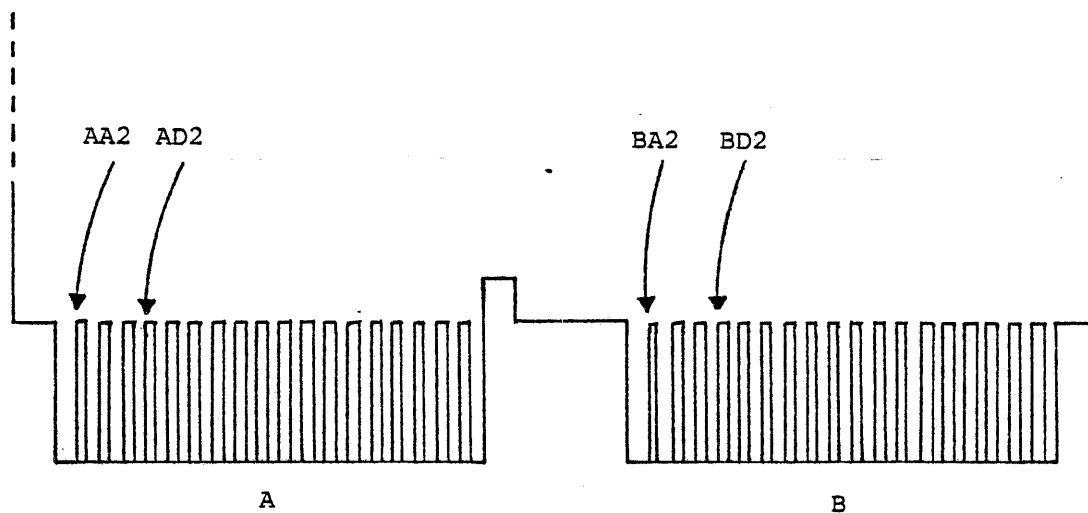


Figure 2-3: Solder Side 2

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# Section 3

## Functional Description

### 3.0 ACCESS TIME

The read access time of the PM-SV32A is 250ns typical. Access time is defined as the time from when BDIN or BDOUT is asserted to the time BRPLY is asserted.

### 3.1 CYCLE TIME

The cycle time of the memory is 500ns typical. Cycle time is defined as the time from when a BDIN or BDOUT is asserted to the time when the memory is ready to accept another BDIN or BDOUT.

### 3.2 REFRESH ELECTRONICS

The PM-SV32A memory module uses 16K and 8K MOS dynamic random access memory devices. These devices, being dynamic, require refreshing. The refresh sequence is a series of forced memory read (DATI) operations where only the row addresses are significant.

The PM-SV32A offers the user two switch selectable modes of refresh. The first mode of refresh is entirely under the control of either processor microcode, or an external user selected DMA device, such as the PM-REV11. In this mode, all 128 rows of all dynamic MOS memory chips in an LSI-11 system are sequentially refreshed. The timing specification of 8K and 16K RAMs require refresh cycles twice as often as 4K RAMs. Therefore, a double refresh cycle is performed on the PM-SV32A when a bus refresh is initiated. Consequently, the PM-SV32A takes longer to do a bus refresh (850ns) and must be the memory used for refresh reply.

The second refresh mode is accomplished on the PM-SV32A memory board by on-board refresh circuitry. In this mode, the PM-SV32A generates a double refresh cycle at a periodic rate of approximately 30 $\mu$ s. That is, every 30 $\mu$ s the memory is disabled and refreshed at the refresh counter address contained on the PM-SV32A. If a processor request is generated while a refresh cycle is in progress, the request is stored and accomplished immediately following the refresh cycle.

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On the other hand, if a 30µs refresh request occurs while the memory is in a processor request cycle, the refresh request is stored and accomplished following the processor cycle. The PM-SV32A refresh is transparent to the processor.

### 3.3 ADDRESS SELECTION

The memory module is address selectable on 4K boundaries. The address of the memory module may begin on any 4K boundary and end on any 4K boundary depending upon the memory size. Addresses are selected using DIP switch settings. Tables 2-2 and 2-3 list the DIP switch settings. The PM-SV32A can also respond to addresses in the I/O page via switch 3. The I/O page addressing available is 29K, 30K, and 31K.

### 3.4 MODES OF OPERATION

The PM-SV32A is capable of operating in five different modes. The modes are:

DATI (Read Cycle): In this mode, the memory reads data from a specified location and presents this data to the data bus.

DATO (Write Cycle): In this mode, the memory writes new data from the data bus into a specified location in memory.

DATOB (Write Byte Cycle): In this mode, the memory performs a write on a specified byte of data. The other byte of data is not affected.

DATIO/DATIOB (Read Modify Write): In this mode, the memory performs two memory cycles. A read (DATI) followed by either a DATO or DATOB operation specified by the processor.

Refresh Cycle: In this mode, the memory performs a memory refresh cycle as described in Section 3.2.

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### 3.5 INTERFACE

The memory interfaces with the processor and peripherals via card edge connectors on the bottom of the memory card. Pin connections for these connectors are listed in Table 3-1. All receivers present one bus load to the data bus and comply with DEC LSI-11 bus receiver specifications. Input/output signals required for memory operations are shown below.

MEMORY CONNECTOR SECTION A				MEMORY CONNECTOR SECTION B			
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
J1	GND	A2	+5V	B1	BPOK H	A2	+5V
		C2	GND			C2	GND
		D2	+12V			D2	+12V
		E2	BDCOUT L			E2	BDAL 2 L
		F2	BRPLY L			F2	BDAL 3 L
		H2	BDIN L			H2	BDAL 4 L
M1	GND	J2	BSYNC L	J1	GND	J2	BDAL 5 L
		K2	BWTBT L			K2	BDAL 6 L
R1	BREF L	M2	BIAKO L	M1	GND	L2	BDAL 7 L
		N2	BIAKI L			M2	BDAL 8 L
		P2	BBST L			N2	BDAL 9 L
		R2	BDMGI L			P2	BDAL10 L
S1	+12B	S2	BDMGO L	T1	GND	R2	BDAL11 L
T1	GND	T2	BINIT L			S2	BDAL12 L
V1	+5VB	U2	BDAL 0 L	V1	+5V	T2	BDAL13 L
		V2	BDAL 1 L			U2	BDAL14 L
						V2	BDAL15 L

NOTE: Q bus signals not connected on the memory are not listed.

Table 3-1: PM-SV32A Backplane Interface Connection

- BDAL00-BDAL15 - 16 address and bidirectional data bus lines on which address and data are time multiplexed.
- BPOKL - Used by memory to enable refresh oscillator during power up.
- BRPLY - Response line from memory indicating to processor that the memory is through with data for either a read or write cycle.
- BREFL - Control line enabling all memories to do a refresh cycle.
- BDIN - Control line from the processor to the memory which enables a read cycle.

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- BDOU - Control line from the processor to the memory which enables a write cycle.
- BWTBT - Control line from the processor to the memory which enables a write byte cycle.
- BREF - Control line from the processor to the memory which initiates a refresh cycle.
- BBS7L - Control line from the processor to the memory which normally causes deselection of the memory in the 28 - 32K range.

### 3.6 QUALITY ASSURANCE

This section provides an overview of the quality standard designed into Plessey Peripheral Systems products.

#### 3.6.1 Design Standards

The materials, fabrication, and workmanship conform to the best commercial practices. Specifically, the following standards are met:

1. Printed circuit boards are gold plated on the connector fingers.
2. Silicon integrated circuits in dual in-line packages unless their application is prohibited by voltage swing, power dissipation or function availability.
3. All assemblies having the same part number are interchangeable.
4. The circuits are designed to minimize the risk of catastrophic failure propagation.
5. All hardware items of the products are resistant to corrosion.
6. All components are suitably derated for maximum MTBF (mean time between failures).

#### 3.6.2 Quality and Workmanship

Workmanship is consistent with the best commercial computer practices.

#### 3.6.3 Reliability and Maintainability

Plessey Peripheral Systems products are designed for high reliability and maintainability, as well as low cost and state-of-the-art electrical performance.

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- Mean Time Between Failures (MTBF)

Each product is designed and components chosen to yield the maximum MTBF. MTBF calculations based on MIL-STD-217-A are available for specific products.

- Mean Time To Repair (MTTR)

The products are designed with the objective of rapid fault isolation and repair. The degree of internal system modularity is maximized such that all systems within their design limits can be constructed from a minimum variety of printed circuit boards. Complete systems are mounted when possible on one circuit board assembly.

- Routine Maintenance

Most products are designed to require no routine maintenance or adjustment to achieve satisfactory operation.

#### 3.6.4 Service Life

The memory products are designed for a service life of ten years at 24 hours per day exclusive of time required for periodic routine maintenance.

#### 3.6.5 Warranty

All Plessey solid state products are warrantied for a period of six months, including parts and labor.

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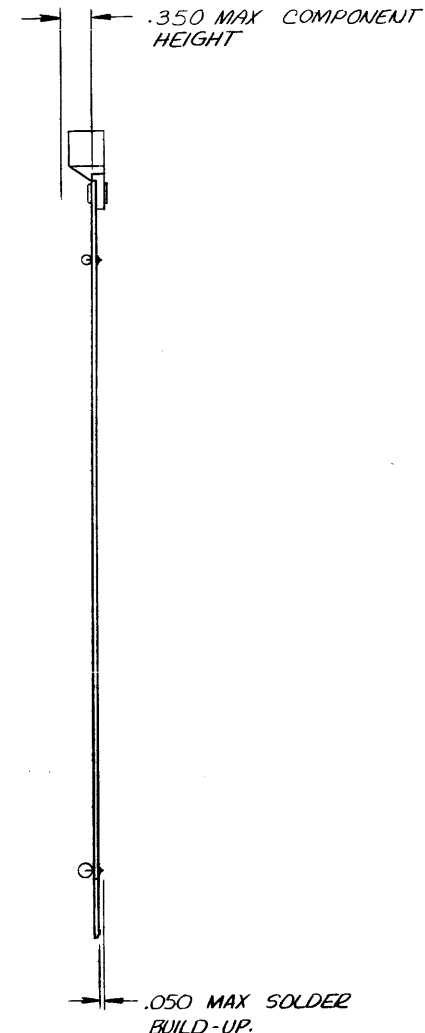
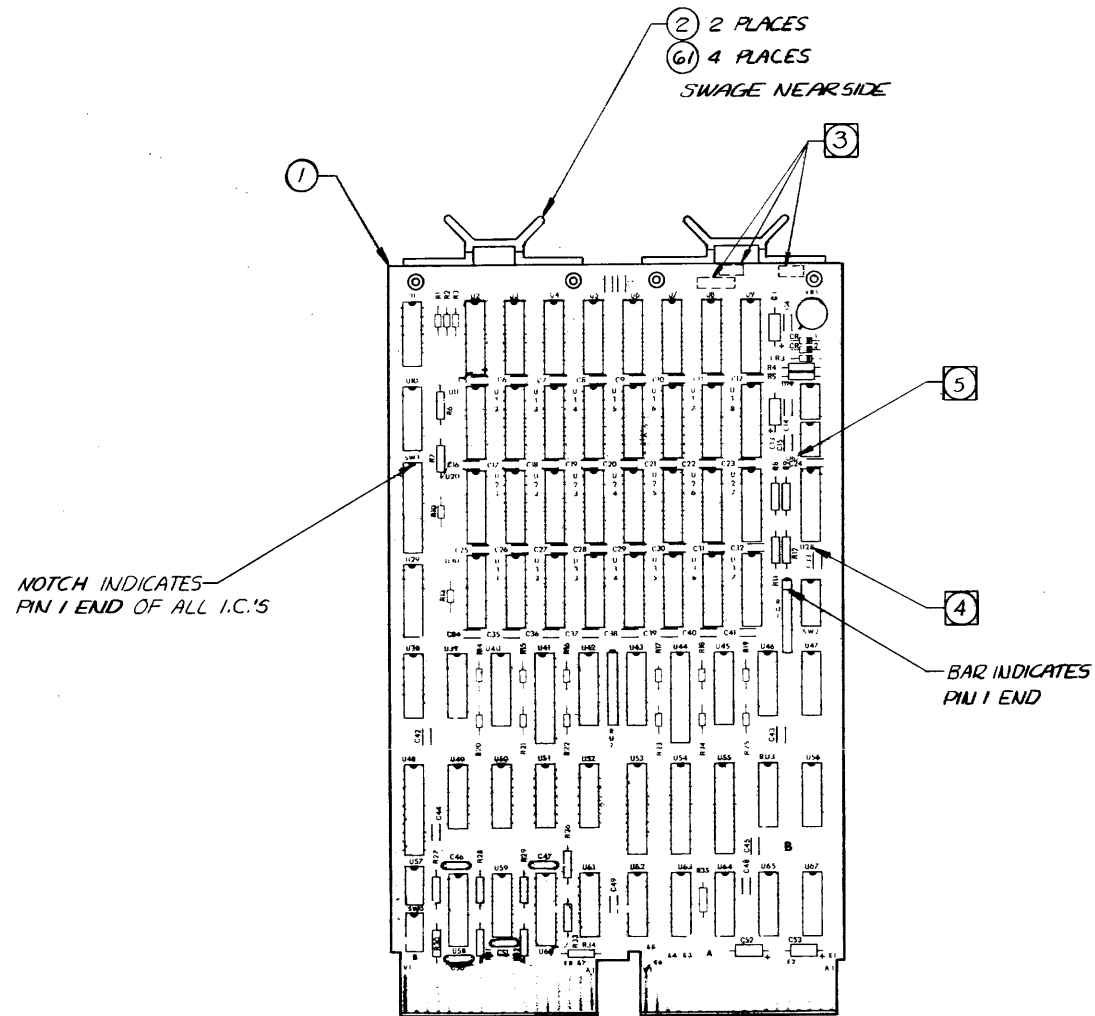
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REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED
A	REL TO PROD PER E02413	9-21-78	[Signature]



FOR BATTERY BACKUP OPTION  
MODIFY ASSEMBLY AS FOLLOWS:

- ISOLATE THE FOLLOWING BY CUTTING THE CIRCUIT ETCH BETWEEN:

CONN. PIN	E#
AD2	E2
BD2	E8
AA2	E1
BA2	E7
- ADD THE FOLLOWING JUMPERS USING 20 AWG WIRE

E2	TO	E3
E8	TO	E4
E1	TO	E5
E7	TO	E6

**PRODUCTION RELEASE**

- 5 U67 SHOULD BE U68
  - 4 COMPONENT DESIGNATIONS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON PART.
  - 3 MARK ASSEMBLY VERSION NUMBER, LATEST ASSEMBLY REVISION LETTER AND SERIAL NUMBER USING BLACK INK, PER MIL-M-13231, GROUP III. LOCATION APPROXIMATELY AS SHOWN.
2. FOR SCHEMATIC DIAGRAM SEE 5D701660.  
1. ASSEMBLE AND INSPECT PER WORKMANSHIP STANDARDS MANUAL.
- NOTES: UNLESS OTHERWISE SPECIFIED

PART ASSY NO. & QTY PER ASSY	PARTS LIST	NOMENCLATURE OR DESCRIPTION / MATERIAL	SPEC SOURCE	CODE IDENT NO.	FIND NO.
X		FOR PARTS LIST SEE PL701660-103			5
X		FOR PARTS LIST SEE PL701660-102			4
X		FOR PARTS LIST SEE PL701660-101			3
X		FOR PARTS LIST SEE PL701660-100			2
					1

DO NOT SCALE DRAWING	CONTRACT NO.	Plessey Memories Incorporated
SCREW THREADS PER HANDBOOK 11-28 COUNTERBORE AND SPOTFACE FILLET RADI TO BE 60 MAXIMUM REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO 60R ROUGHNESS OF MACHINED SURFACES 125/ PER USAS 5141	DRAWN L. LAMBERT 4-24-78 CHECK L. Frankis 4-28-78 ENGR PROJ. ENGR [Signature] 4-28-78 PROD. DESIGNER [Signature] 4-24-78	Sta Ana, California
STANDARD HOLE TOLERANCE PER AND 5057 TOLERANCES ON DIM. IN. .0005 - .0015 ANGLES .01 - .02	OTHER [Signature]	
INTERPRET DIMENSIONS AND TOLERANCES PER USAS 7143 DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH UNLESS OTHERWISE SPECIFIED	APPROVALS	

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SCALE: FULL SHEET 1 OF 1

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<b>PARTS LIST</b>		<b>Plessey Microsystems</b>		REV LTR <b>A</b>
BOARD ASSY, MEMORY, 28K x 16 FM-SV 32A		PL701660-100	CODE IDENT NO. 52648	SH 1 OF 7
REV LTR <b>A</b>		PL701660-100	CODE IDENT NO. 52648	SH 1 OF 7

LTR	DESCRIPTION	DATE	APPROVED
A	REL TO PRODEO 2413	8-21-78	<i>[Signature]</i>

**PRODUCTION RELEASE**

REV STATUS OF SHEETS	REV LTR	A	A	A	A	A	A	A	A	A	A	A	A	A	A
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<b>PARTS LIST</b>	<b>Plessey Microsystems</b>	CODE IDENT NO. 52648	PARTS LIST NO. PL701660-100	SH 2	REV LTR <b>A</b>
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REFERENCE DESIGNATION	F I N O D	REFERENCE DESIGNATION	F I N O D	REFERENCE DESIGNATION	F I N O D
CR 1-3	7	U41,44,48,53-55	29	C46	52
VR 1	8	U52	30	C50	53
SW 1	9	U57	31	C4,15	54
SW 2	10	U19, 68	32	C14,24	55
SW 3	11		33	C 1,2,5-12,16-23,25-	56
	12	R1-3,10,13-25	34	41	
	13	R12	35	C13	57
	14	R5	36	C53	58
112-9,11-18,20-27,30-37		R6,7,34	37	C3,52	59
U64,65	15	R9	38	C42,43,44,45,48,49	60
U40,42,43,45	16	R4,11	39		
U50	17	R26-28	40	LAB SET:	
U10,47,51,56	18	R32	41	R8,29-31,33	
U63	19	R35	42	C47	
U49	20		43		
U1	21		44		
U67	22		45		
U38,39	23		46		
U62	24	RU2	47		
U59,61	25	RU3	48		
U46	26	RU1	49		
U58,60	27		50		
U29	28	C51	51		

<b>PARTS LIST</b>		<b>Plessey Microsystems</b>		REV LTR <b>A</b>
BOARD ASSY, MEMORY, 28K x 16 FM-SV 32A		PL701660-100	CODE IDENT NO. 52648	SH 3 OF 7

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N O D	S Y M	C/I USAGE
1	701659-01	PRINTED WIRING BOARD				1		
2	701339-100	HANDLE				2		
						3		
						4		
						5		
						6		
3	138000-001	DIODE				7		
1	LM320-H05	VOLTAGE REGULATOR				8		
1	3-435668-0	SWITCH, 10 POS. DIP W/TAPE	AMP			9		
1	3-435668-5	SWITCH, 5 POS. DIP W/TAPE	AMP			10		
1	3-435668-4	SWITCH, 4 POS. DIP	AMP			11		
						12		
						13		

<b>PARTS LIST</b>	<b>Plessey Microsystems</b>	CODE IDENT NO. 52648	PARTS LIST NO. PL701660-100	SH 4	REV LTR <b>A</b>
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QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N O D	S Y M	C/I USAGE
32	136003	I.C./DYNAMIC RAM, 16 K	MDSTEK			14		
2	DS8640	I.C./ QUAD NOR UNIFIED BUS RECEIVER	NATIONAL			15		
4	DS8641	I.C./ QUAD UNIFIED BUS TRANSCEIVER	NATIONAL			16		
1	SN7400	I.C./ QUAD 2-INPUT POS-NAND GATE	T. I.			17		
4	SN74S00	I.C./ QUAD 2-INPUT POS-NAND GATE	T. I.			18		
1	SN74S04	I.C./ HEX INVERTER	T. I.			19		
1	SN7408	I.C./ QUAD 2-INPUT POS AND GATE	T. I.			20		
1	SN74S08	I.C./ QUAD 2-INPUT POS AND GATE	T. I.			21		
1	SN74S10	I.C./ TRIPLE 3-INPUT POS-NAND GATE	T. I.			22		
2	SN7432	I.C./ QUAD 2-INPUT POS-OR GATE	T. I.			23		
1	SN7438	I.C./ QUAD 2-INPUT POS-NAND BUFFER W/O	T. I.			24		
2	SN74S74	I.C./ DUAL D-TYPE POS-EDG-TRIG F/F W/PRESET/CLEAR	T. I.			25		
1	SN7486	I.C./ QUAD 2-INPUT EXCLSYE-OR GATE	T. I.			26		

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CODE IDENT NO. DWG NO. PL 701660-100  
 SIZE **B** SCALE REV A SHEET 1 OF 2  
 Form 000087

PARTS LIST		Plessey Microsystems		CODE IDENT NO.	PARTS LIST NO.	SH	REV LTR	C/I USAGE											
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I CODE	INV ON HAND	P A R	UNIT COST								
2	SN74123	I.C./ DUAL RETRIG MONO MULTI W/CLEAR	T.1.			27													
1	SN74156	I.C./ DUAL 2 LINE TO 4 LINE DEC / DEMULTI	T.1.			28													
6	SN74S373	I.C./ OCTAL D-TYPE FLIP - FLOP	T.1.			29													
1	SN74393	I.C./ DUAL 4-BIT DECADE AND BINARY COUNTER	T.1.			30													
1	SN75452	I.C./ DUAL PERIPHERAL POS-NAND DRIVER	T.1.			31													
2	NE555	TIMER	NATIONAL			32													
						33													
17	RC05GF330J	RESISTOR, 33Ω, ±5%, 1/8 W	MIL-R-II			34													
1	RC07GF101J	RESISTOR, 100Ω, ±5%, 1/4 W	MIL-R-II			35													
1	RC07GF212J	RESISTOR, 2.7K, ±5%, 1/4 W	MIL-R-II			36													
3	RC07GF412J	RESISTOR, 4.7K, ±5%, 1/4 W	MIL-R-II			37													
1	RC07GF153J	RESISTOR, 15K, ±5%, 1/4 W	MIL-R-II			38													
2	RC07GF223J	RESISTOR, 22K, ±5%, 1/4 W	MIL-R-II			39													

PARTS LIST		Plessey Microsystems		CODE IDENT NO.	PARTS LIST NO.	SH	REV LTR	C/I USAGE											
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I CODE	INV ON HAND	P A R	UNIT COST								
1	CD15FD101J03	CAPACITOR, 100 pf, ±5%, 500V	CORNELL-DUBILIER			53													
2	CK05BX102K	CAPACITOR, .001μf, ±10%, 100V	MIL-C-11015			54													
2	CK05BX103K	CAPACITOR, .01μf, ±10%, 100V	MIL-C-11015			55													
35	CK05BX104K	CAPACITOR, .1μf,	MIL-C-11015			56													
1	150D474X0035A2	CAPACITOR, .47μf, 35V	SPRAGUE			57													
	150D475X0010A2	CAPACITOR, .47μf, 10V, ±20%	SPRAGUE			58													
2	150D225X0020A2	CAPACITOR, 2.2μf, 20V, ±20%	SPRAGUE			59													
6	CGA103ZDZ	CAPACITOR, .01μf, 50V	UNITRODE			60													
4	MS16535-154	RIVET / TUBULAR, OVAL HD .123 DIA x .188 LG				61													

PARTS LIST		Plessey Microsystems		CODE IDENT NO.	PARTS LIST NO.	SH	REV LTR	C/I USAGE											
QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	CODE IDENT NO.	ZONE	F I N D	S Y M	C/I CODE	INV ON HAND	P A R	UNIT COST								
3	RC07GF273J	RESISTOR, 27K, ±5%, 1/4 W	MIL-R-II			40													
1	RC07GF333J	RESISTOR, 33K, ±5%, 1/4 W	MIL-R-II			41													
1	RC07GF102J	RESISTOR, 1KΩ, ±5%, 1/4 W	MIL-R-II			42													
						43													
						44													
						45													
						46													
1	750-83-R33Ω	RESISTOR MODULE, 33Ω	CTS			47													
1	760-3-R39Ω	RESISTOR MODULE, 39Ω	CTS			48													
1	750-81-R4.7K	RESISTOR MODULE, 4.7K	CTS			49													
						50													
1	CD15FD220J03	CAPACITOR, 22 pf, ±5%, 500V	CORNELL-DUBILIER			51													
1	CD15FD470J03	CAPACITOR, 47 pf, ±5%, 500V	CORNELL-DUBILIER			52													

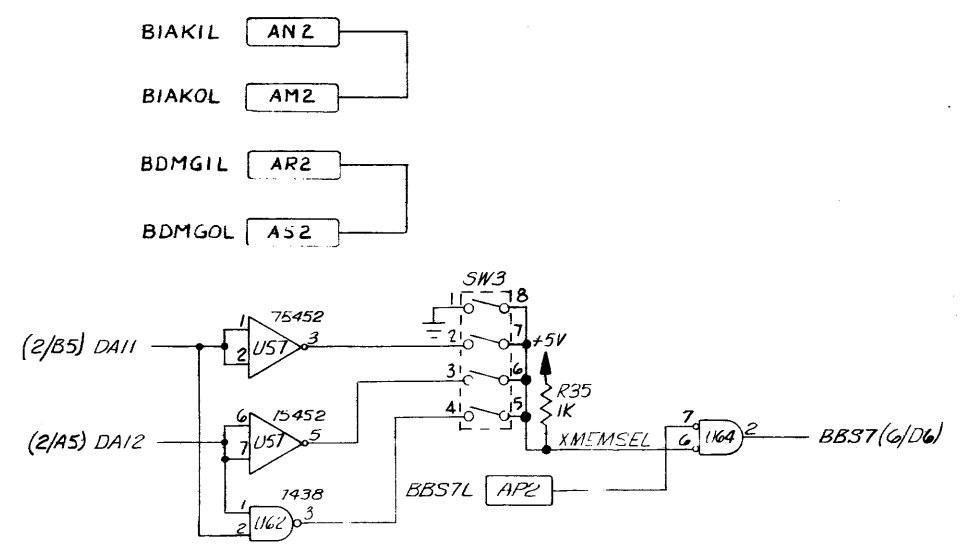
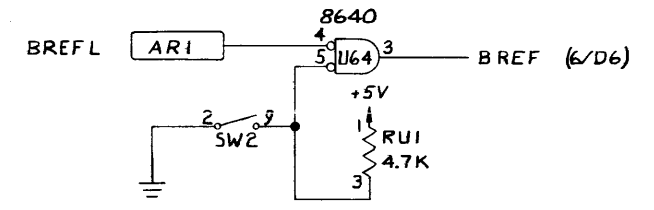
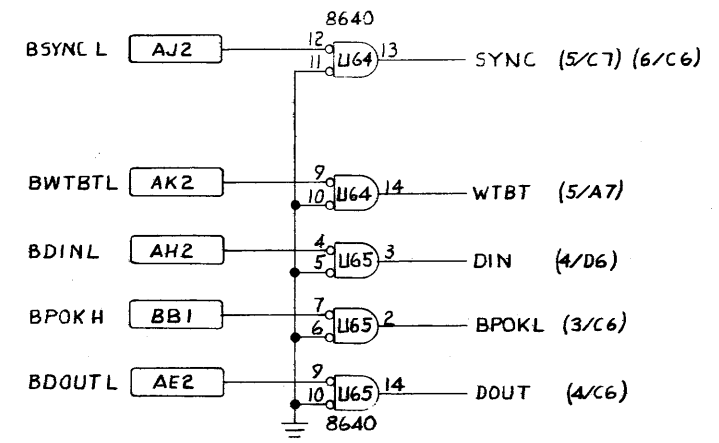
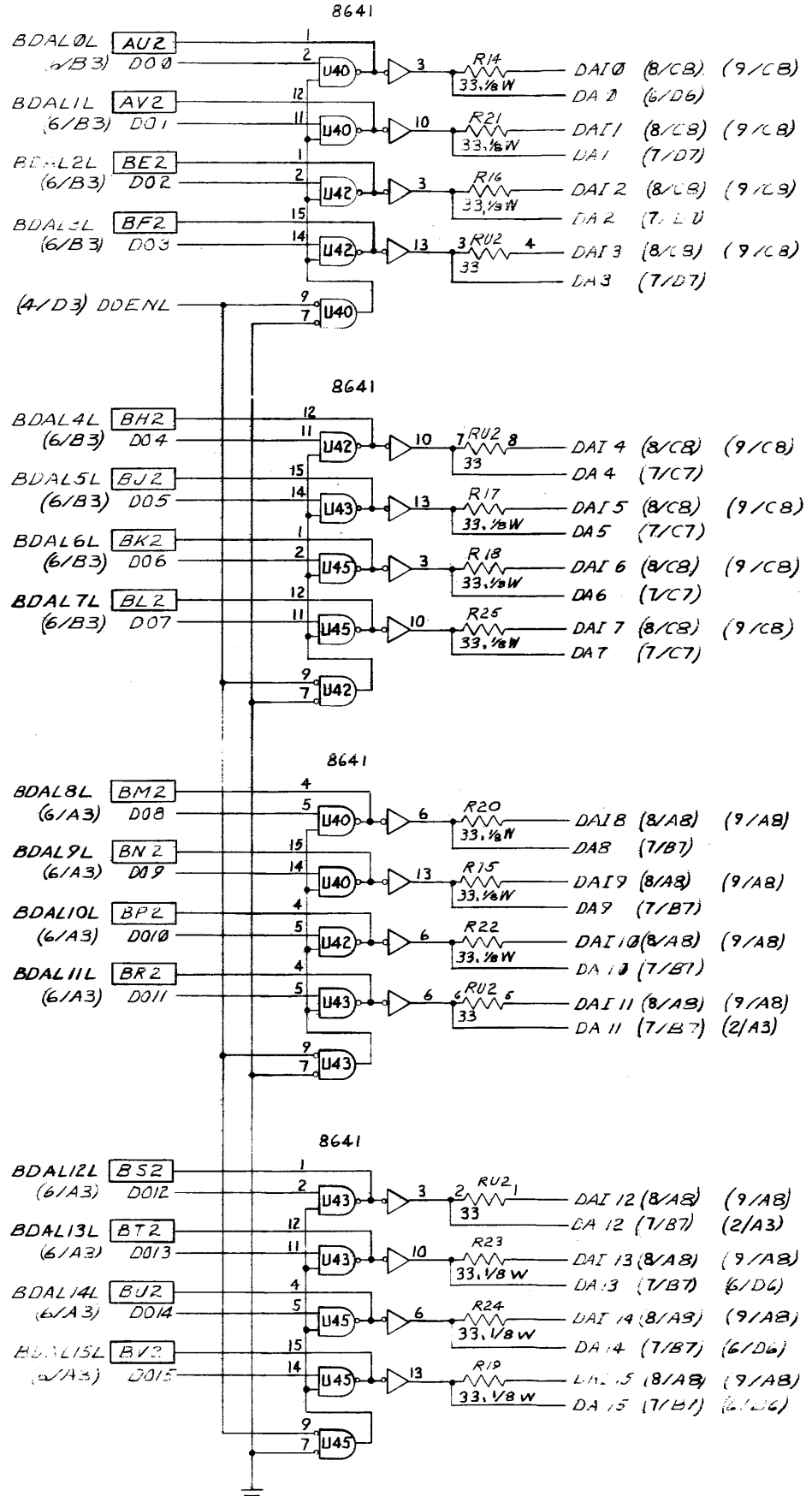
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 SCALE    REV A    SHEET 2 OF 2



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SIZE	CODE IDENT NO.	DWG NO.
D	52649	SD701660
SCALE	REV B	SHEET 2 OF 9
		DISTR NO.

8

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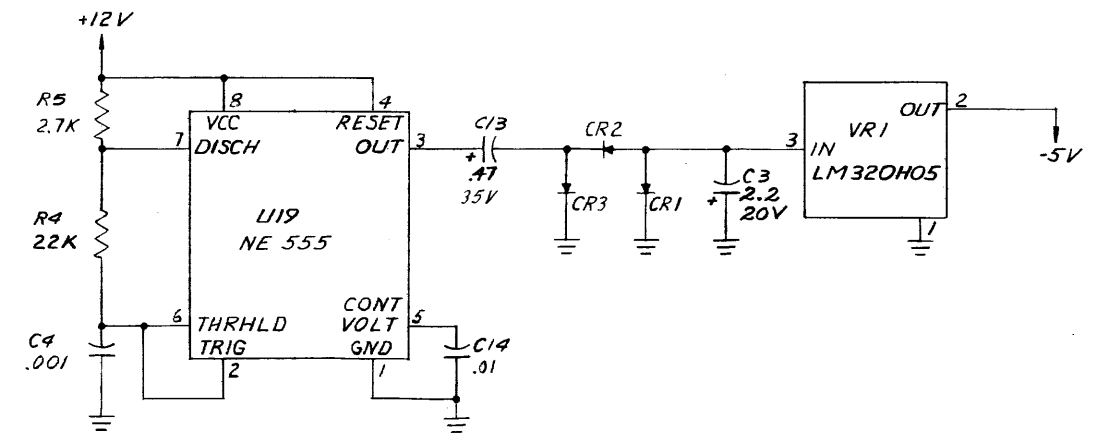
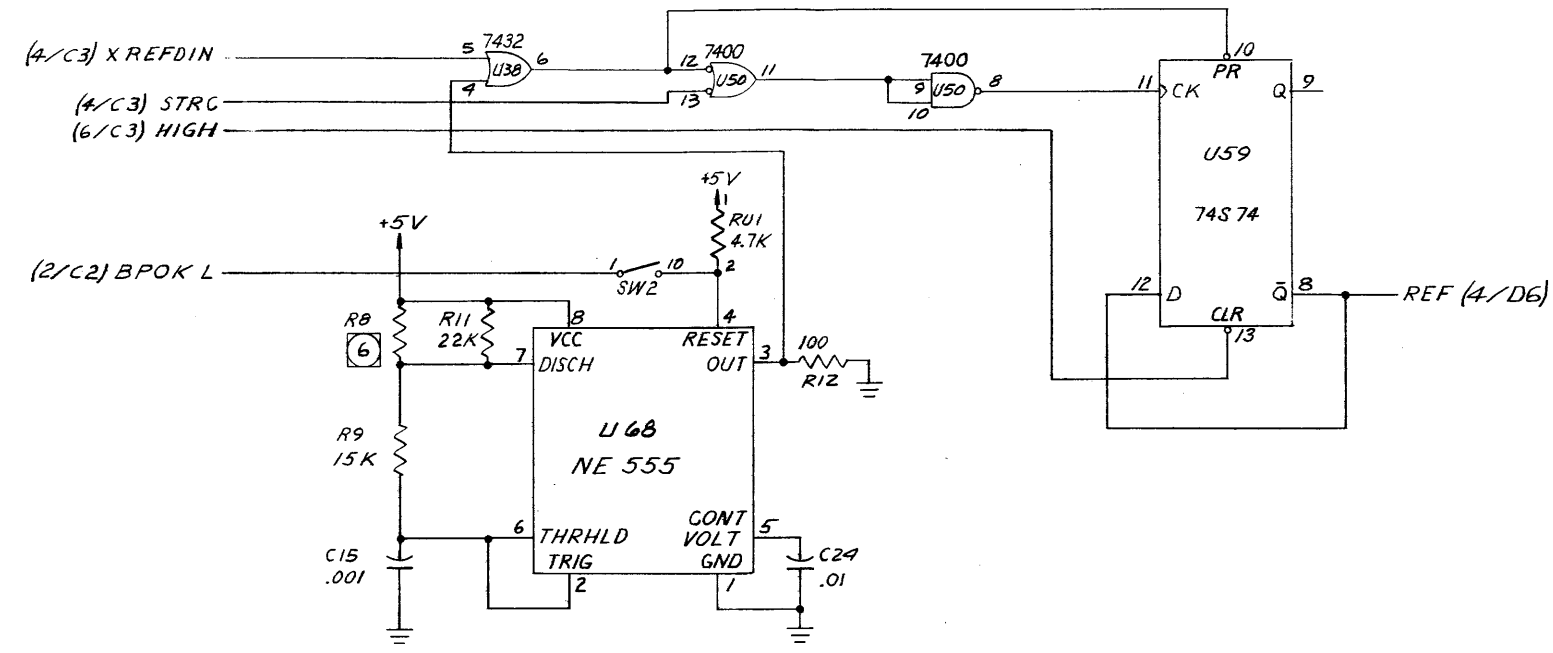
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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



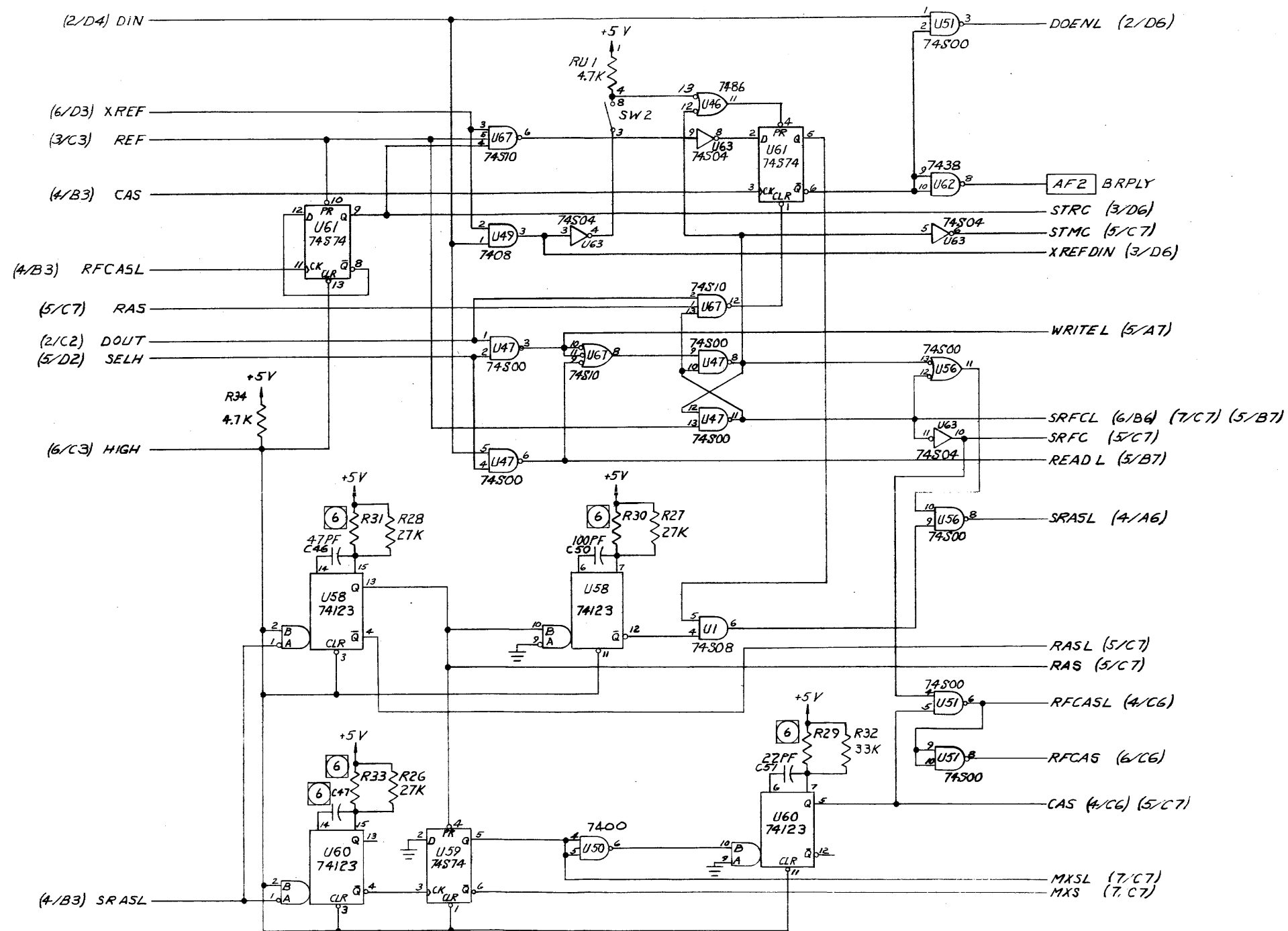
SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701660
SCALE	REV	SHEET 3 OF 9
	B	

SD701660

C-4

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REVISIONS				
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		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
D	52E45	SD701660
SCALE: -	REV B	SHEET 4 OF 9
		DISTR NO.

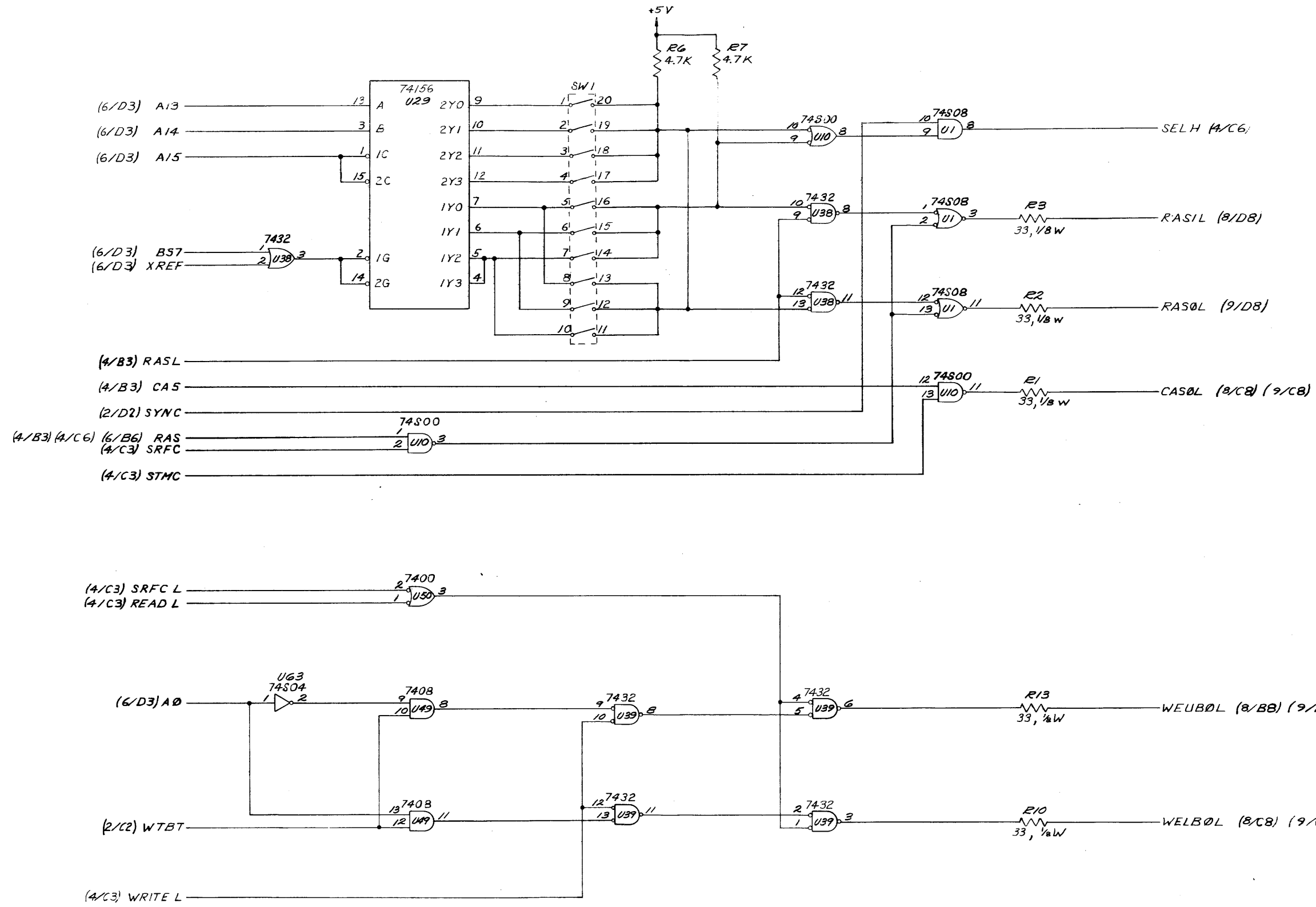
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05



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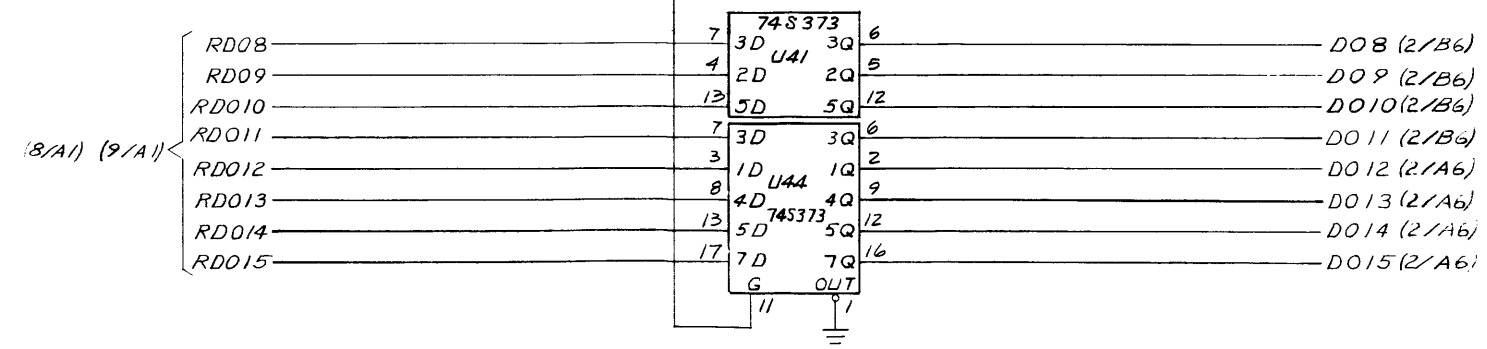
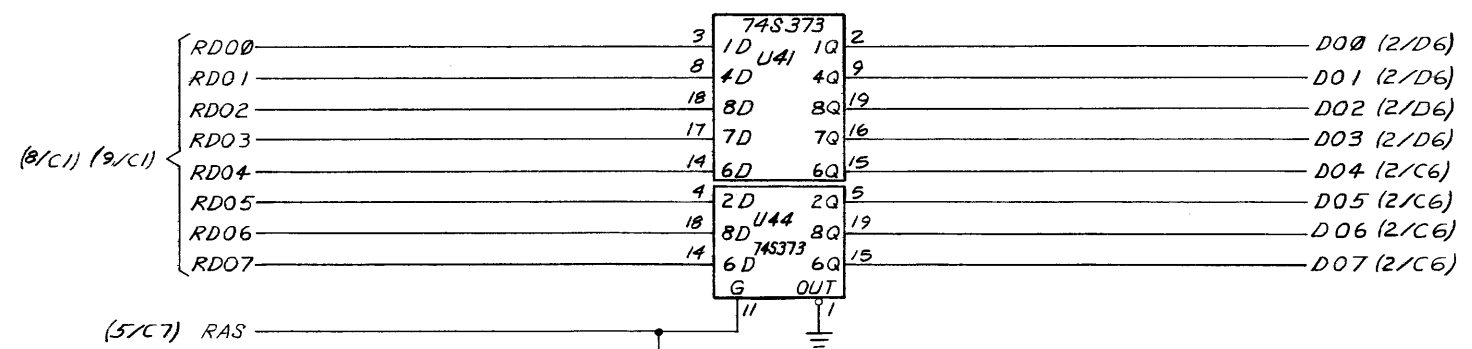
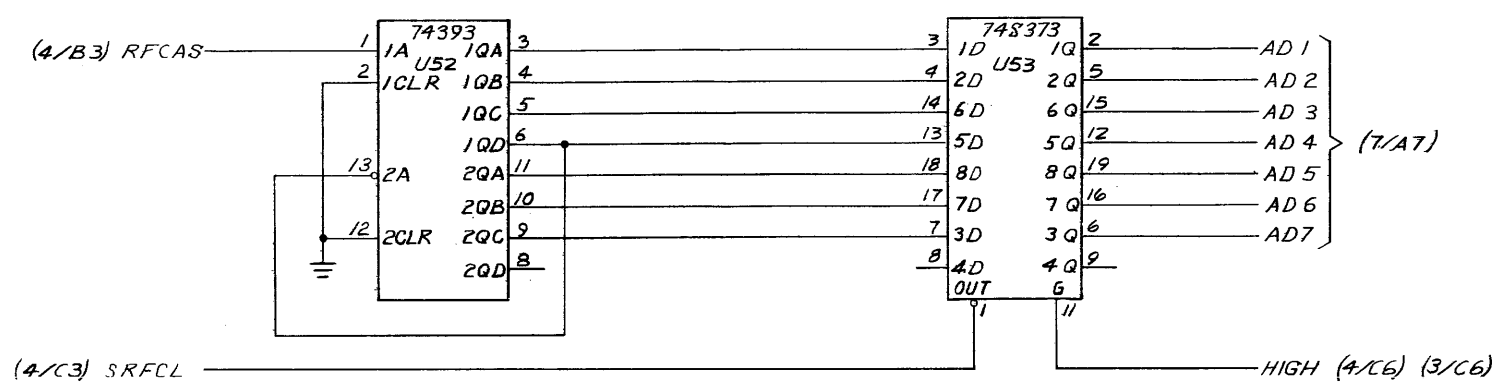
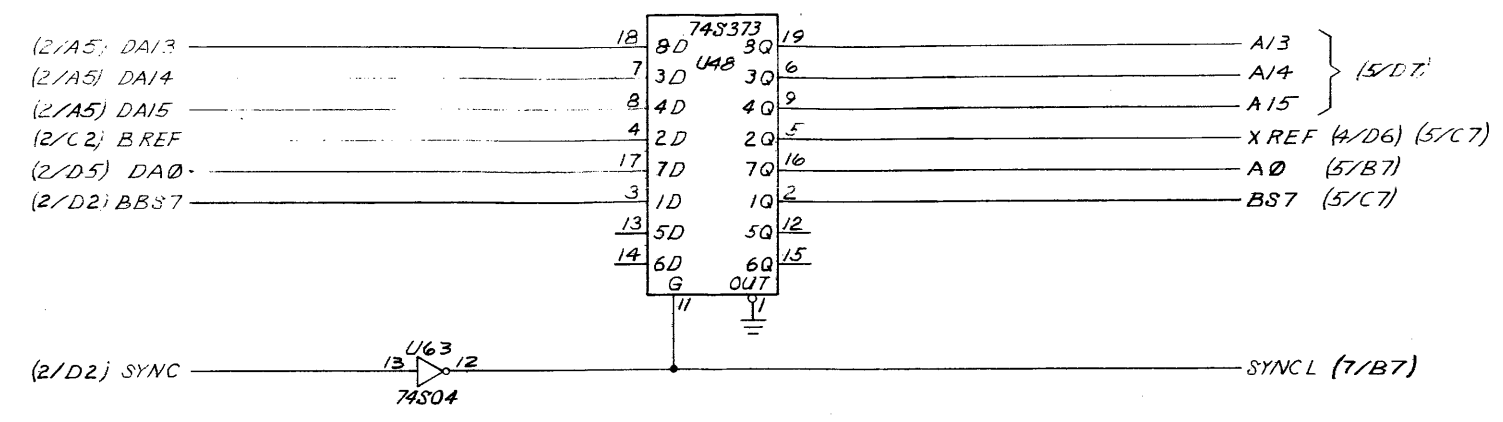
SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701660
SCALE	REV B	SHEET 5 OF 9
		DISTR NO.

SD701660

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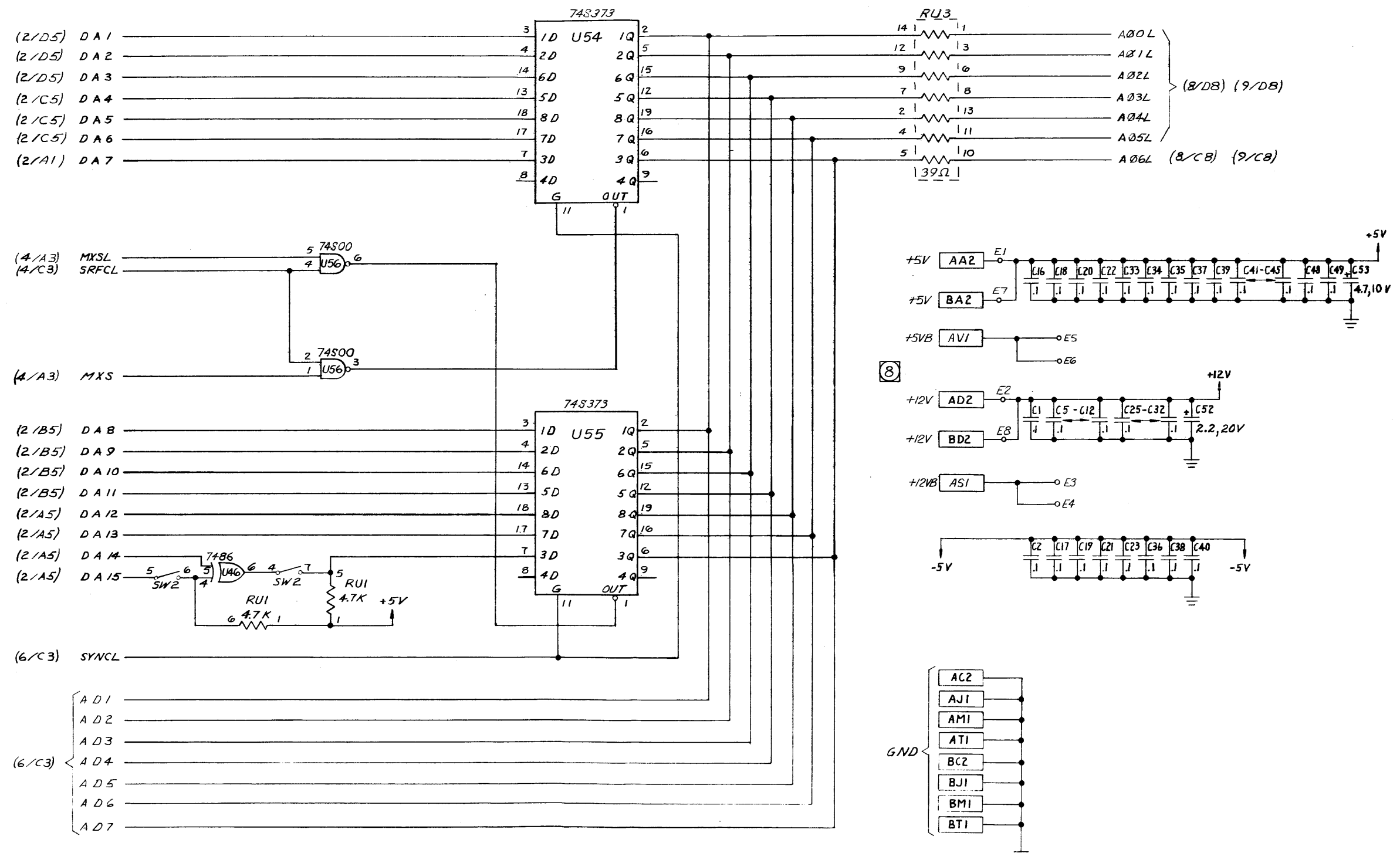
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



SIZE	CODE IDENT NO.	DWG NO.
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SCALE: -	REV B	SHEET 6 OF 9
DISTR NO.		

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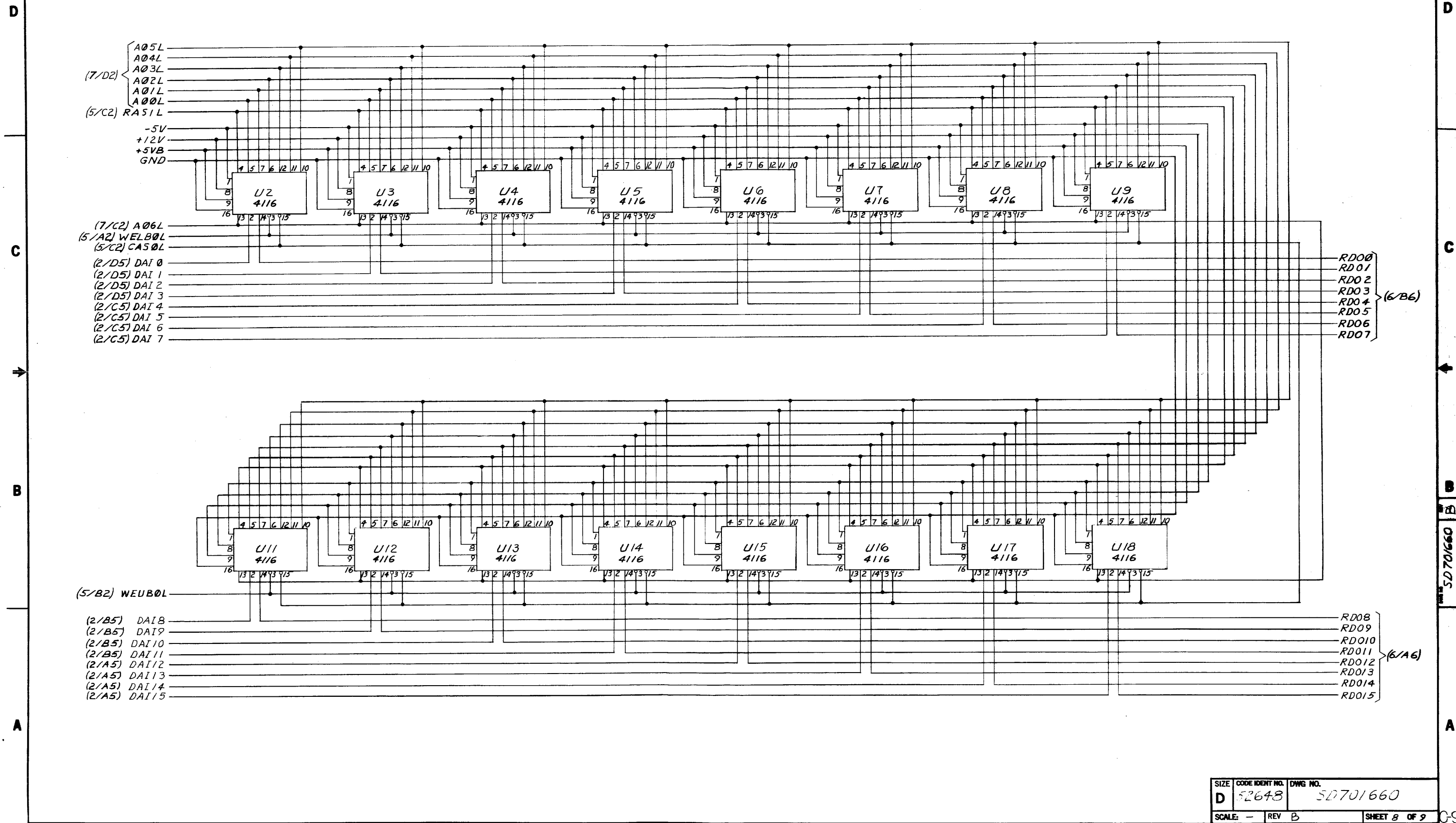
SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD 701660
SCALE: -	REV B	SHEET 7 OF 9
DISTR NO.		

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ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHEET		



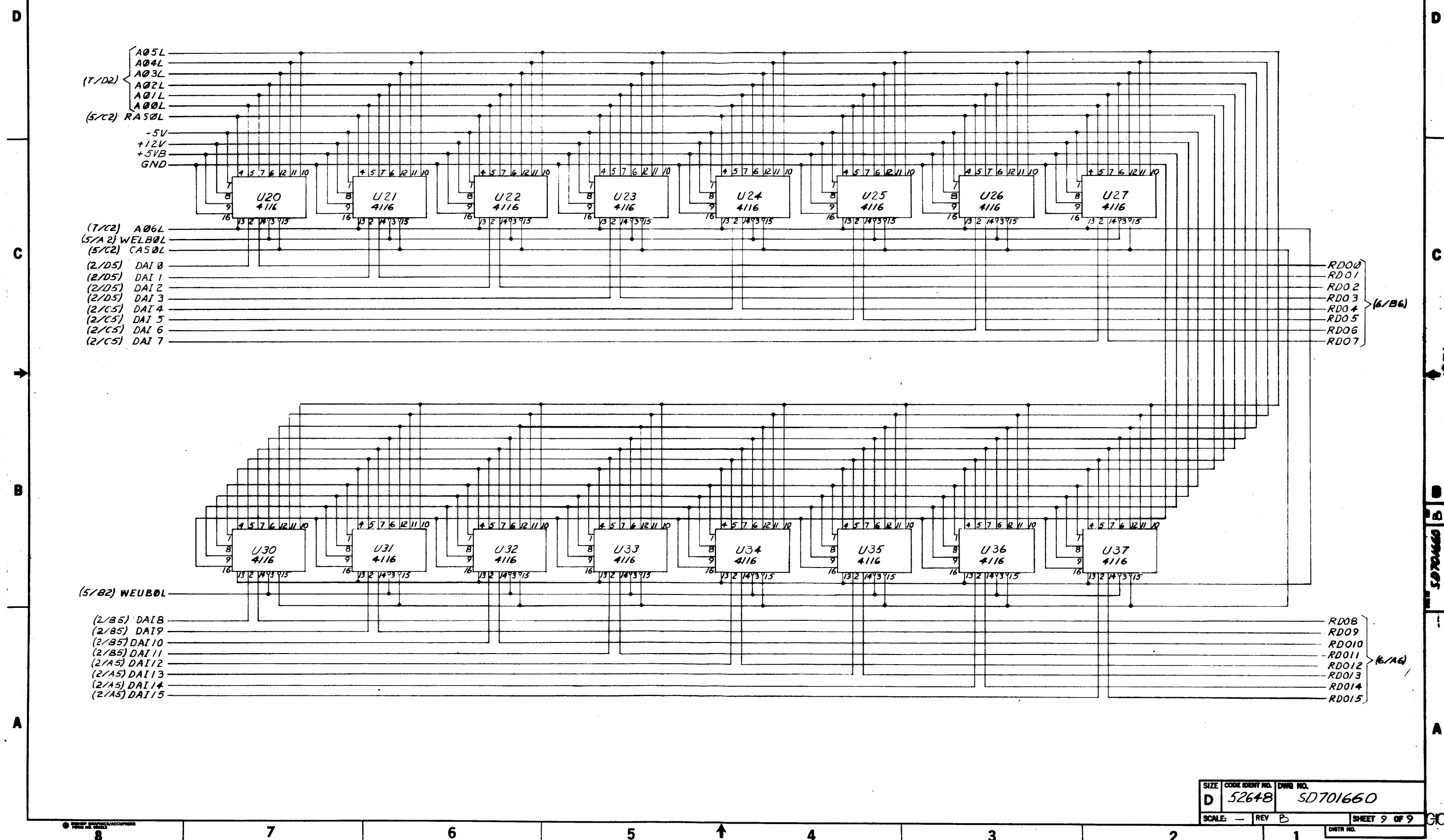
SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701660
SCALE	REV B	SHEET 8 OF 9

SD701660

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SIZE	CODE IDENT NO.	DWG NO.
D	52648	SD701660
SCALE	REV B	SHEET 9 OF 9
		DISTR NO.

5070660 [B] 5070660 [A]

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